## **CLAIMS**

-	~		
ı		aım	٠

1	1.	A method comprising:		
2		delaying a first clock signal to produce a delayed clock signal;		
3		measuring time intervals between phases of the first clock signal; and		
4		adjusting the delayed clock signal based on the time intervals.		
1	2.	The method of claim 1, further comprising:		
2		generating the first clock signal from an input clock signal, wherein the first		
3	clock	signal includes first pulses, which correspond to leading edges of the input		
4	clock	signal, and second pulses, which correspond to falling edges of the input clock		
5	signa	1.		
1	3.	The method of claim 2, wherein measuring the time intervals comprises:		
2		determining a first duty cycle skew of the first clock signal by adjusting a		
3	time (	delay between the first clock signal and the delayed clock signal; and		
4		comparing the first clock signal and the delayed clock signal.		
1	4.	The method of claim 3, wherein determining the first duty cycle skew		
2	comp	rises:		
3		adjusting the time delay to a first value, which indicates a first time delay		
4	when	a first delayed pulse of the delayed clock signal occurs in proximity to a		
5	secon	d pulse of the first clock signal;		
6		adjusting the time delay to a second value, which indicates a second time		
7	delay when a second delayed pulse of the delayed clock signal occurs in proximity			
Q	to a first pulse of the first clock signal: and			

- 9 determining the first duty cycle skew based on the first time delay and the 10 second time delay.
- 1 5. The method of claim 3, wherein adjusting the delayed clock signal
- 2 comprises:
- producing a third clock signal with a second duty cycle skew, wherein the
- 4 second duty cycle skew is less than the first duty cycle skew by a time difference
- 5 that is based on the first duty cycle skew.
- 1 6. A method comprising:
- 2 generating a first clock signal from an input clock signal, wherein the first
- 3 clock signal includes first pulses, which correspond to leading edges of the input
- 4 clock signal, and second pulses, which correspond to falling edges of the input clock
- 5 signal;
- delaying the first clock signal by a time delay to produce a delayed clock
- 7 signal having first delayed pulses and second delayed pulses;
- 8 determining a first duty cycle skew of the first clock signal by adjusting the
- 9 time delay and comparing the first clock signal and the delayed clock signal; and
- producing a third clock signal with a second duty cycle skew, wherein the
- second duty cycle skew is less than the first duty cycle skew by a time difference
- that is based on the first duty cycle skew.
- 1 7. The method of claim 6, wherein determining the first duty cycle skew
- 2 comprises:
- adjusting the time delay to a first value, which indicates a first time delay
- 4 when a first delayed pulse of the delayed clock signal occurs in proximity to a
- 5 second pulse of the first clock signal;
- 6 adjusting the time delay to a second value, which indicates a second time

- 7 delay when a second delayed pulse of the delayed clock signal occurs in proximity
- 8 to a first pulse of the first clock signal; and
- 9 determining the first duty cycle skew based on the first time delay and the
- 10 second time delay.
- 1 8. The method of claim 6, wherein producing the third clock signal comprises:
- 2 calculating a skew adjustment value as approximately one half of a
- difference between the first time delay and the second time delay; and
- 4 applying the skew adjustment value to a clock signal to produce the third
- 5 clock signal.
- 1 9. An apparatus comprising:
- a delay element, which functions to delay a first clock signal to produce a
- delayed clock signal;
- a detector, operatively coupled to the delay element, which functions to
- 5 measure time intervals between phases of the first clock signal based on
- 6 comparisons between the first clock signal and the delayed clock signal; and
- a control element, operatively coupled to the detector, which functions to
- 8 adjust the delayed clock signal based on the time intervals.
- 1 10. The apparatus of claim 9, further comprising:
- a clock generator, which functions to generate the first clock signal from an
- 3 input clock signal, wherein the first clock signal includes first pulses, which
- 4 correspond to leading edges of the input clock signal, and second pulses, which
- 5 correspond to falling edges of the input clock signal.
- 1 11. The apparatus of claim 10, wherein the detector functions to measure the
- 2 time intervals by:

3	determining a first duty cycle skew of the first clock signal by adjusting a		
4	time delay between the first clock signal and the delayed clock signal; and		
5	comparing the first clock signal and the delayed clock signal.		
1	12. An apparatus comprising:		
2	a clock generator, which functions to generate a first clock signal from an		
3	input clock signal, wherein the first clock signal includes first pulses, which		
4	correspond to leading edges of the input clock signal, and second pulses, which		
5	correspond to falling edges of the input clock signal;		
6	a delay element, operatively coupled to the clock generator, which functions		
7	to delay the first clock signal by a time delay to produce a delayed clock signal		
8	having first delayed pulses and second delayed pulses; and		
9	a first circuit, operatively coupled to the delay element, which functions to		
10	determine a first duty cycle skew of the first clock signal by adjusting the time delay		
11	and comparing the first clock signal and the delayed clock signal, and which further		
12	functions to provide control information for producing a third clock signal with a		
13	second duty cycle skew, wherein the second duty cycle skew is less than the first		
14	duty cycle skew by a time difference that is based on the first duty cycle skew.		
1	13. The apparatus of claim 12, wherein the first circuit determines the first duty		
2	cycle skew by:		
3	adjusting the time delay to a first value, which indicates a first time delay		
4	when a first delayed pulse of the delayed clock signal occurs in proximity to a		
5	second pulse of the first clock signal;		
6	adjusting the time delay to a second value, which indicates a second time		
7	delay when a second delayed pulse of the delayed clock signal occurs in proximity		
8	to a first pulse of the first clock signal; and		

Docket No. 884.993US2 P9565C

9

determining the first duty cycle skew based on the first time delay and the

- 10 second time delay.
- 1 14. The apparatus of claim 12, wherein the first circuit provides the control
- 2 information by:
- 3 calculating a skew adjustment value as approximately one half of a
- 4 difference between the first time delay and the second time delay; and
- 5 applying the skew adjustment value to a clock signal to produce the third
- 6 clock signal.
- 1 15. A microprocessor comprising:
- a delay element, which functions to delay a first clock signal to produce a
- 3 delayed clock signal;
- a detector, operatively coupled to the delay element, which functions to
- 5 measure time intervals between phases of the first clock signal based on
- 6 comparisons between the first clock signal and the delayed clock signal; and
- a control element, operatively coupled to the detector, which functions to
- 8 adjust the delayed clock signal based on the time intervals.
- 1 16. The microprocessor of claim 15, further comprising:
- a clock generator, which functions to generate the first clock signal from an
- 3 input clock signal, wherein the first clock signal includes first pulses, which
- 4 correspond to leading edges of the input clock signal, and second pulses, which
- 5 correspond to falling edges of the input clock signal.
- 1 17. The microprocessor of claim 16, wherein the detector functions to measure
- 2 the time intervals by:
- determining a first duty cycle skew of the first clock signal by adjusting a
- 4 time delay between the first clock signal and the delayed clock signal; and

Docket No. 884.993US2 P9565C

5 comparing the first clock signal and the delayed clock signal. 1 18. A microprocessor comprising: 2 a clock generator, which functions to generate a first clock signal from an 3 input clock signal, wherein the first clock signal includes first pulses, which 4 correspond to leading edges of the input clock signal, and second pulses, which 5 correspond to falling edges of the input clock signal; 6 a delay element, operatively coupled to the clock generator, which functions 7 to delay the first clock signal by a time delay to produce a delayed clock signal having first delayed pulses and second delayed pulses; and 8 9 a first circuit, operatively coupled to the delay element, which functions to 10 determine a first duty cycle skew of the first clock signal by adjusting the time delay 11 12

and comparing the first clock signal and the delayed clock signal, and which further functions to provide control information for producing a third clock signal with a second duty cycle skew, wherein the second duty cycle skew is less than the first duty cycle skew by a time difference that is based on the first duty cycle skew.

19. The microprocessor of claim 18, wherein the first circuit determines the first duty cycle skew by:

adjusting the time delay to a first value, which indicates a first time delay when a first delayed pulse of the delayed clock signal occurs in proximity to a second pulse of the first clock signal;

adjusting the time delay to a second value, which indicates a second time delay when a second delayed pulse of the delayed clock signal occurs in proximity to a first pulse of the first clock signal; and

9 determining the first duty cycle skew based on the first time delay and the 10 second time delay.

13

14

1

2

3

4

5

6

7

8

- 1 20. The microprocessor of claim 18, wherein the first circuit provides the control
- 2 information by:
- 3 calculating a skew adjustment value as approximately one half of a
- 4 difference between the first time delay and the second time delay; and
- 5 applying the skew adjustment value to a clock signal to produce the third
- 6 clock signal.